FIG. 1

PRIOR ART

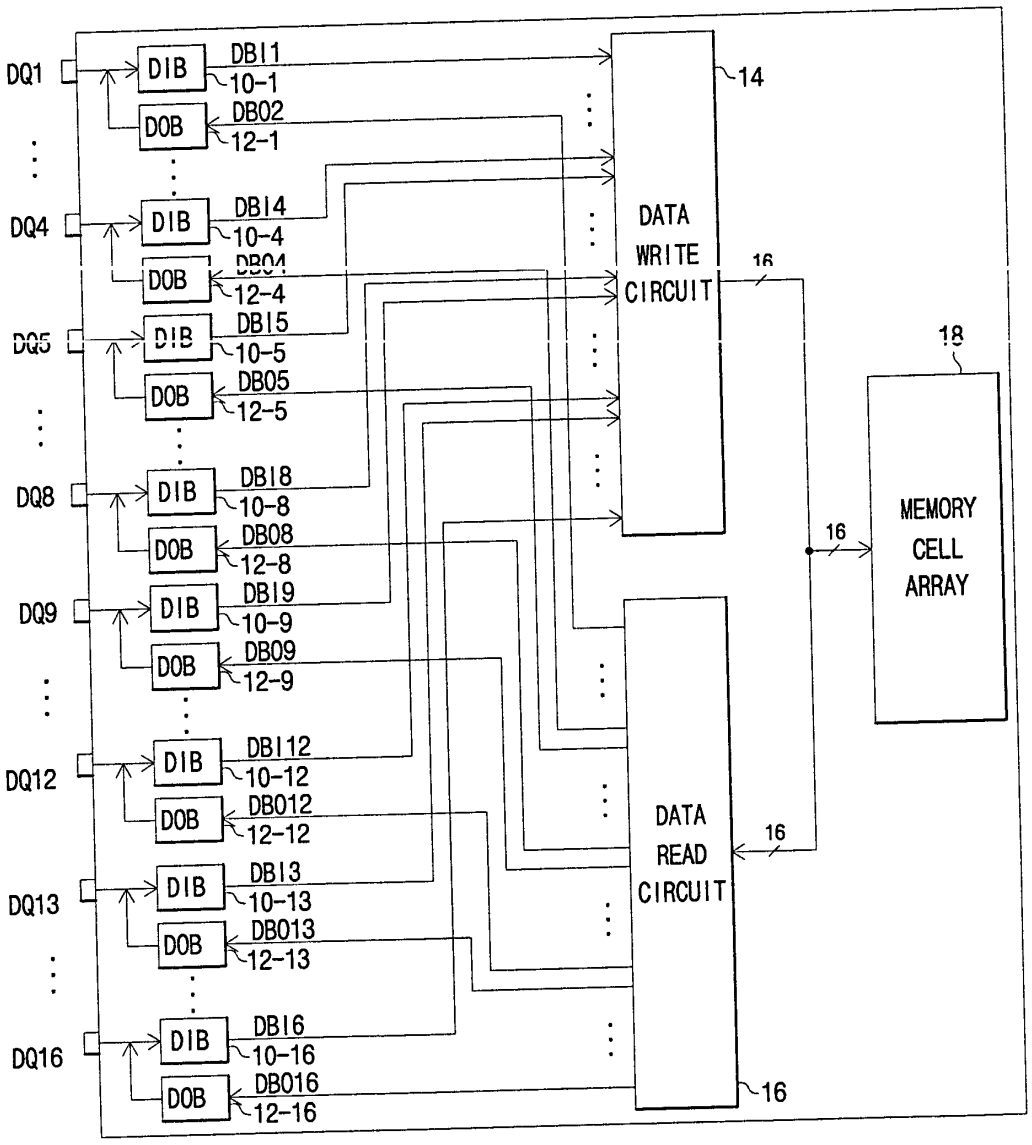


FIG. 2

PRIOR ART

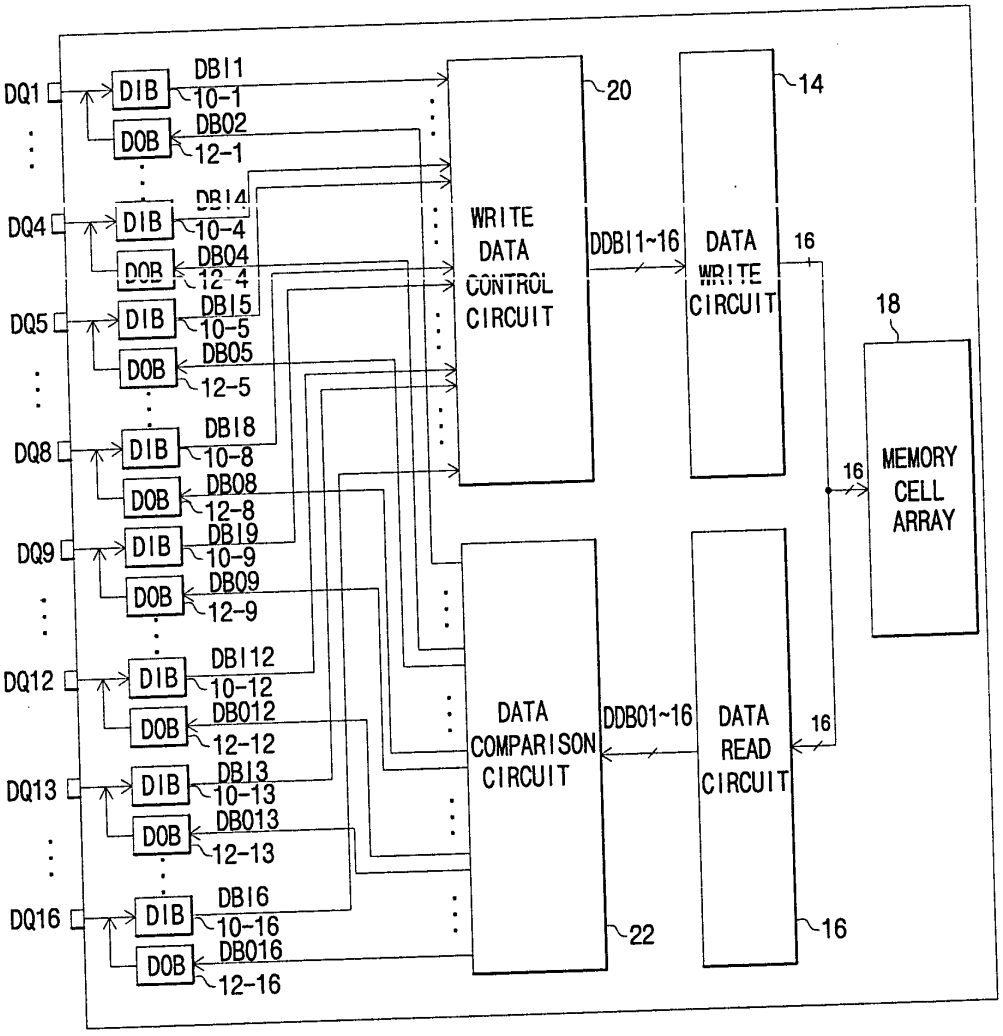


FIG. 3

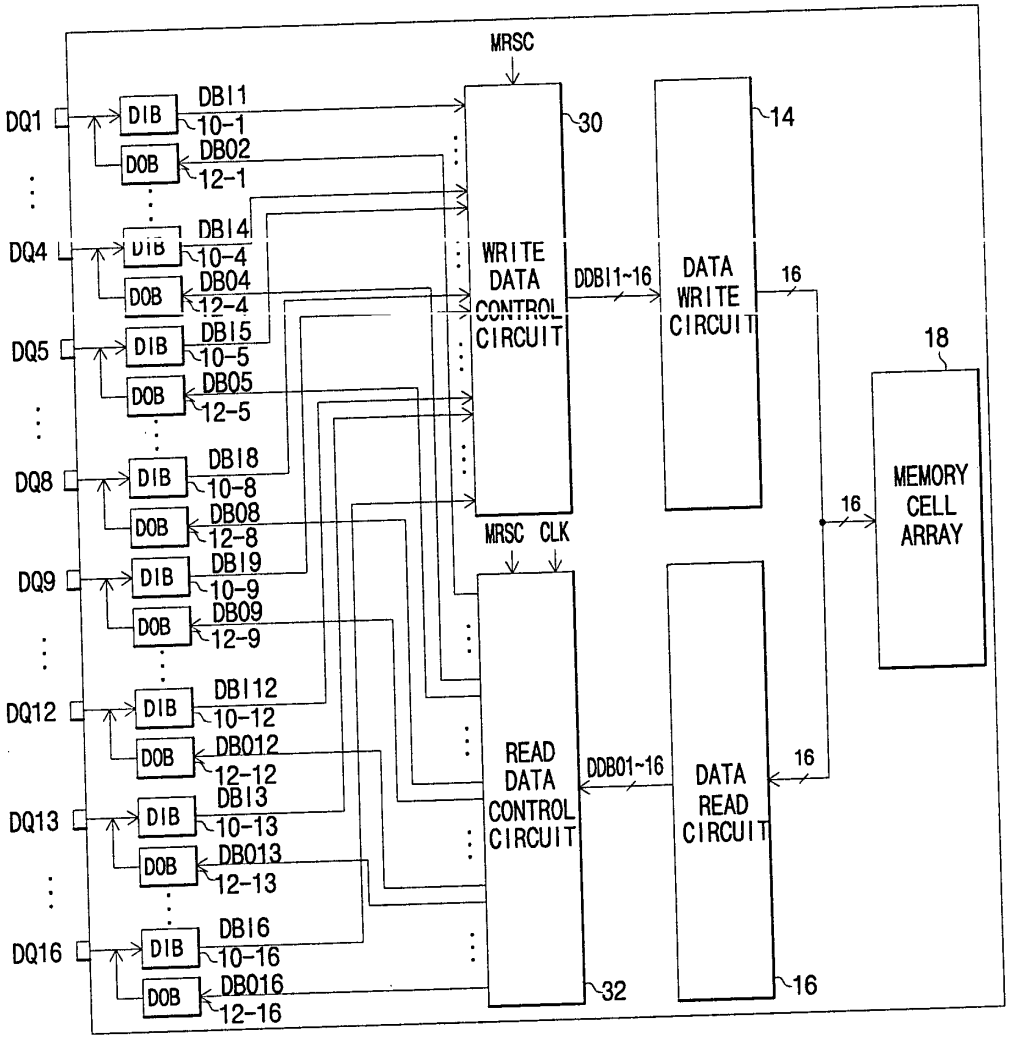

MRSC
DQ1
DIB
DOB
DBI1
10-1
DBO2
12-1
DQ4
DBI4
10-4
DBO4
12-4
DQ5
DBI5
10-5
DBO5
12-5
DQ8
DBI8
10-8
DBO8
12-8
DQ9
DBI9
10-9
DBO9
12-9
DQ12
DBI12
10-12
DBO12
12-12
DQ13
DBI3
10-13
DBO13
12-13
DQ16
DBI6
10-16
DBO16
12-16
WRITE DATA CONTROL CIRCUIT
30
DDBI1~16
DATA WRITE CIRCUIT
14
16
18
MEMORY CELL ARRAY
MRSC CLK
READ DATA CONTROL CIRCUIT
32
DDBO1~16
DATA READ CIRCUIT
16

FIG. 4

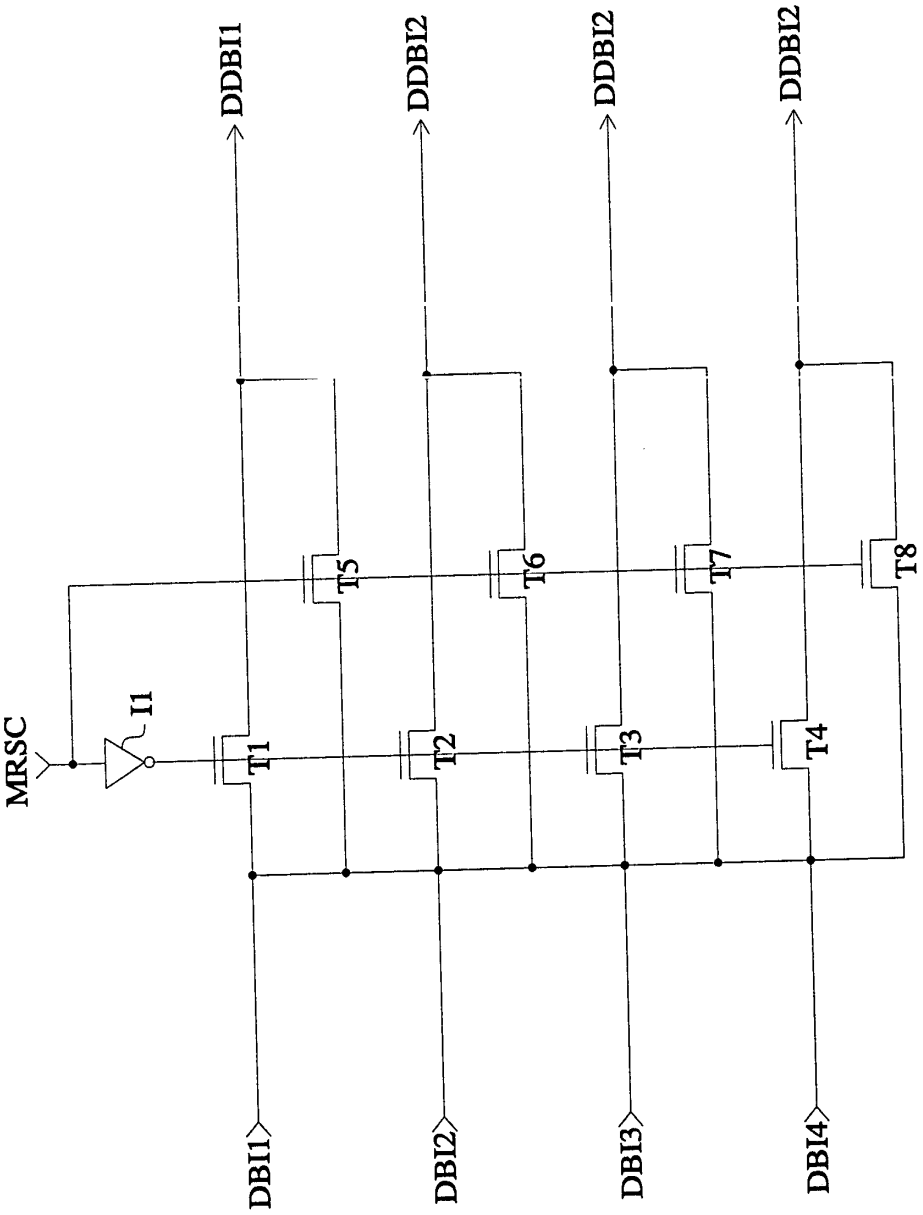
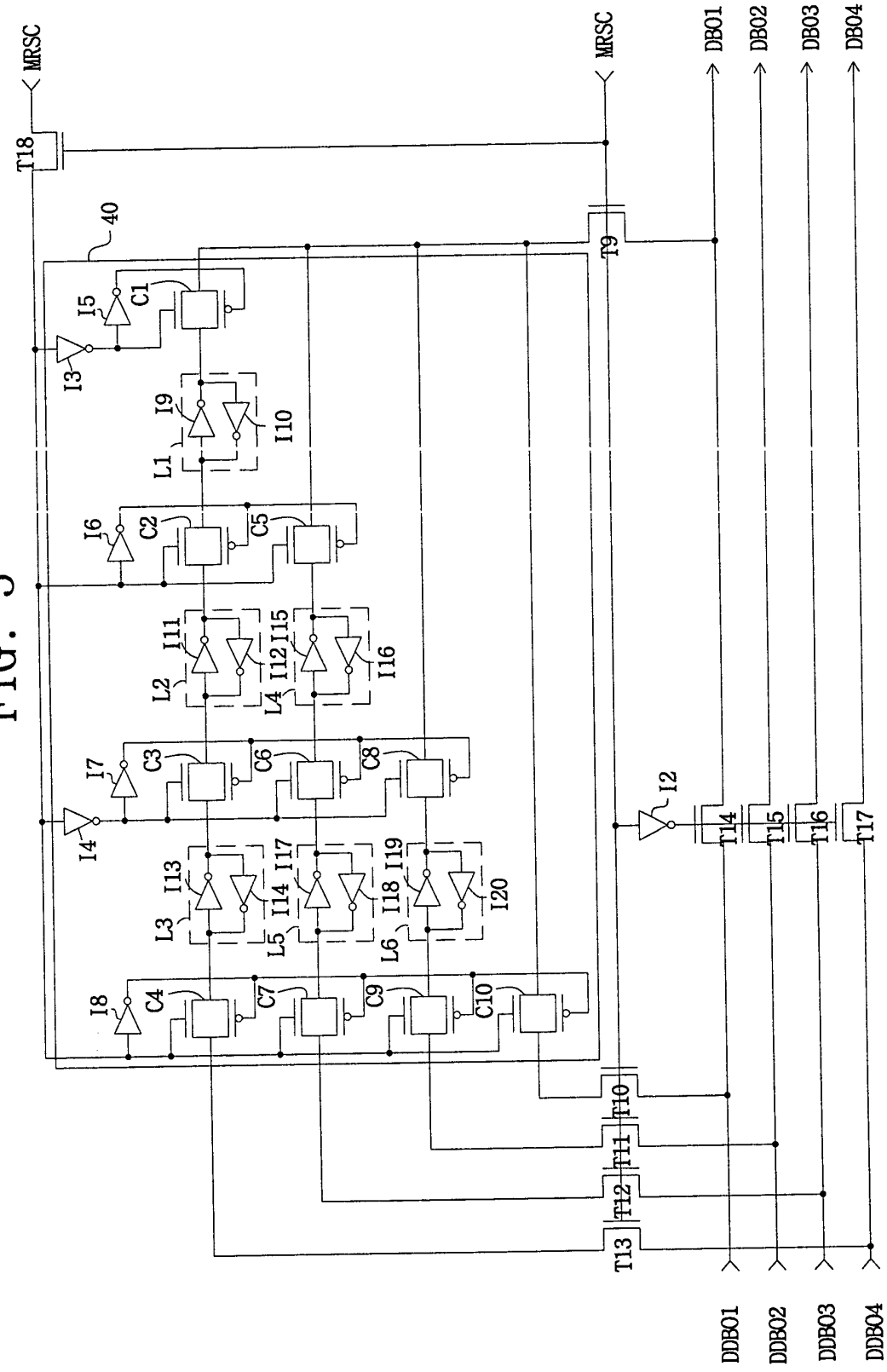

DDBI1
DDBI2
DDBI2
DDBI2
MRSC
I1
T1
T2
T3
T4
T5
T6
T7
T8
DBI1
DBI2
DBI3
DBI4

FIG. 5


MRSC
MRSC
T18
T9
40
DB01
DB02
DB03
DB04
I5
C1
I3
I9
I10
L1
I6
C2
C5
I11
I15
I12
I16
L2
L4
I7
C3
C6
C8
I4
I2
T14
T15
T16
T17
I13
I17
I19
I14
I18
I20
L3
L5
L6
I8
C4
C7
C9
C10
T10
T11
T12
T13
DDB01
DDB02
DDB03
DDB04